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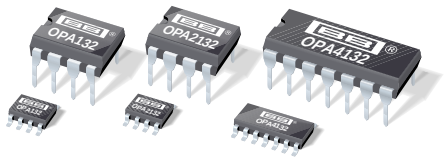


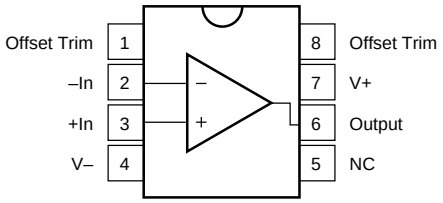
OPA132
OPA2132
OPA4132

High Speed
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

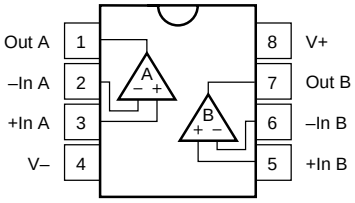
- FET INPUT: I_B = 50pA max
- WIDE BANDWIDTH: 8MHz
- HIGH SLEW RATE: 20V/μs
- LOW NOISE: 8nV/√Hz (1kHz)
- LOW DISTORTION: 0.00008%
- HIGH OPEN-LOOP GAIN: 130dB (600Ω load)
- WIDE SUPPLY RANGE: ±2.5 to ±18V
- LOW OFFSET VOLTAGE: 500μV max
- SINGLE, DUAL, AND QUAD VERSIONS

OPA132



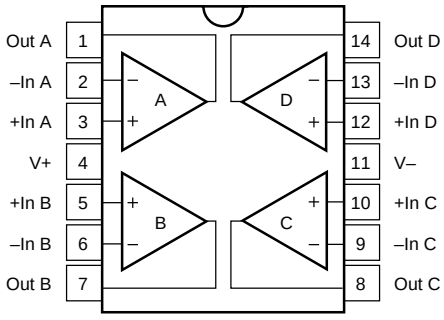
8-Pin DIP, SO-8

OPA2132



8-Pin DIP, SO-8

OPA4132



14-Pin DIP
SO-14

DESCRIPTION

The OPA132 series of FET-input op amps provides high-speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

OPA132 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA132 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1309B Printed in U.S.A. December, 1995

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITION	OPA132P, U OPA2132P, U			OPA132PA, UA OPA2132PA, UA OPA4132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±0.25	±0.5		±0.5	±2	mV
vs Temperature[1]	Operating Temperature Range		±2	±10		*	*	µV/°C
vs Power Supply	V_S = ±2.5V to ±18V		5	15		*	30	µV/V
Channel Separation (dual and quad)	R_L = 2kΩ		0.2			*		µV/V
INPUT BIAS CURRENT								
Input Bias Current[2]	V_{CM} = 0V		+5	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Input Offset Current[2]	V_{CM} = 0V		±2	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			23			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
Current Noise Density, f = 1kHz			3			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–)+2.5	±13	(V+)–2.5	*	*	*	V
Common-Mode Rejection	V_{CM} = –12.5V to +12.5V	96	100		86	94		dB
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode	V_{CM} = –12.5V to +12.5V		10^{13} || 6			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	R_L = 10kΩ, V_O = –14.5V to +13.8V	110	120		104	*		dB
	R_L = 2kΩ, V_O = –13.8V to +13.5V	110	126		104	120		dB
	R_L = 600Ω, V_O = –12.8V to +12.5V	110	130		104	120		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product			8			*		MHz
Slew Rate			±20			*		V/µs
Settling Time: 0.1%	G = –1, 10V Step, C_L = 100pF		0.7			*		µs
0.01%	G = –1, 10V Step, C_L = 100pF		1			*		µs
Overload Recovery Time	G = ±1		0.5			*		µs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms							
	R_L = 2kΩ		0.00008			*		%
	R_L = 600Ω		0.00009			*		%
OUTPUT								
Voltage Output, Positive	R_L = 10kΩ	(V+)–1.2	(V+)–0.9		*	*		V
Negative		(V–)+0.5	(V–)+0.3		*	*		V
Positive	R_L = 2kΩ	(V+)–1.5	(V+)–1.2		*	*		V
Negative		(V–)+1.2	(V–)+0.9		*	*		V
Positive	R_L = 600Ω	(V+)–2.5	(V+)–2.0		*	*		V
Negative		(V–)+2.2	(V–)+1.9		*	*		V
Short-Circuit Current			±40			*		mA
Capacitive Load Drive (Stable Operation)			See Typical Curve			*		
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±4	±4.8		*	*	mA
TEMPERATURE RANGE								
Operating Range		–40		+85	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
14-Pin DIP			80			*		°C/W
SO-14 Surface-Mount			110			*		°C/W

*Specifications same as OPA132P, OPA132U.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at T_J = 25°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit[1]	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
Single		
OPA132PA	8-Pin Plastic DIP	006
OPA132P	8-Pin Plastic DIP	006
OPA132UA	SO-8 Surface-Mount	182
OPA132U	SO-8 Surface-Mount	182
Dual		
OPA2132PA	8-Pin Plastic DIP	006
OPA2132P	8-Pin Plastic DIP	006
OPA2132UA	SO-8 Surface-Mount	182
OPA2132U	SO-8 Surface-Mount	182
Quad		
OPA4132PA	14-Pin Plastic DIP	010
OPA4132UA	SO-14 Surface-Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
Single		
OPA132PA	8-Pin Plastic DIP	–40°C to +85°C
OPA132P	8-Pin Plastic DIP	–40°C to +85°C
OPA132UA	SO-8 Surface-Mount	–40°C to +85°C
OPA132U	SO-8 Surface-Mount	–40°C to +85°C
Dual		
OPA2132PA	8-Pin Plastic DIP	–40°C to +85°C
OPA2132P	8-Pin Plastic DIP	–40°C to +85°C
OPA2132UA	SO-8 Surface-Mount	–40°C to +85°C
OPA2132U	SO-8 Surface-Mount	–40°C to +85°C
Quad		
OPA4132PA	14-Pin Plastic DIP	–40°C to +85°C
OPA4132UA	SO-14 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

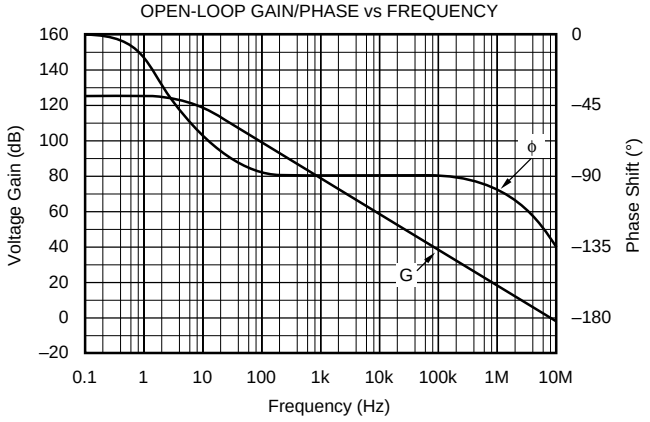
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

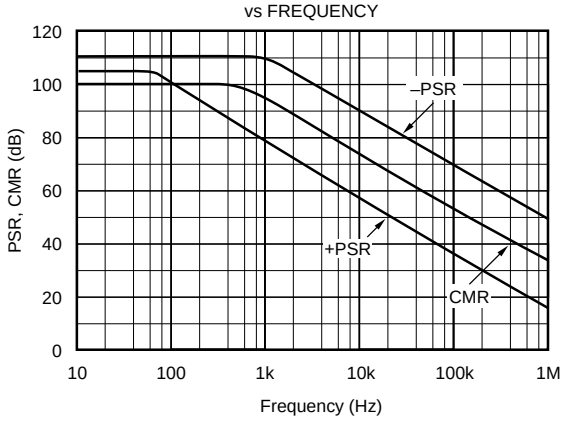
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

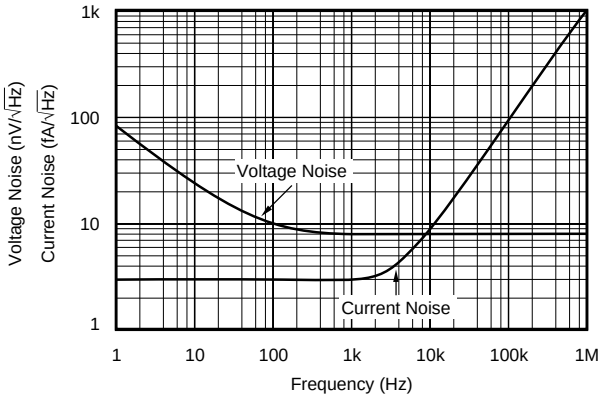
OPEN-LOOP GAIN/PHASE vs FREQUENCY



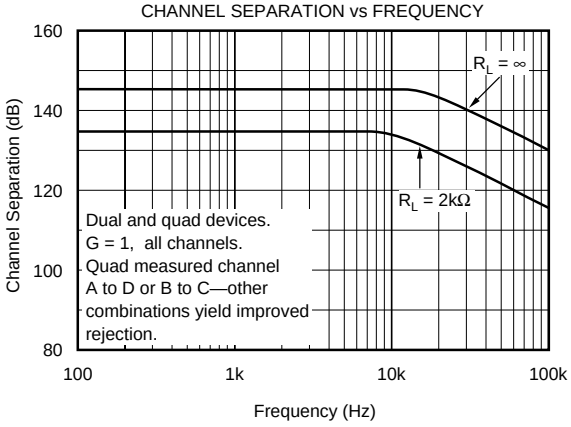
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



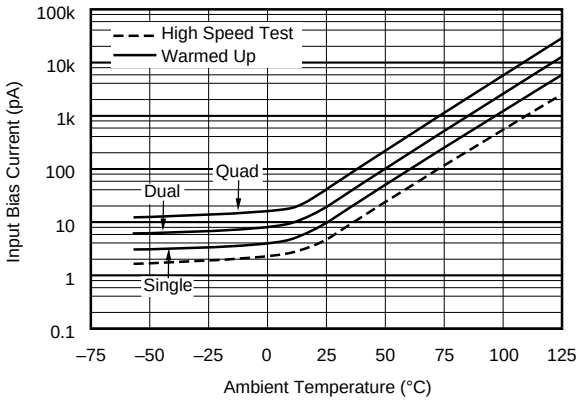
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



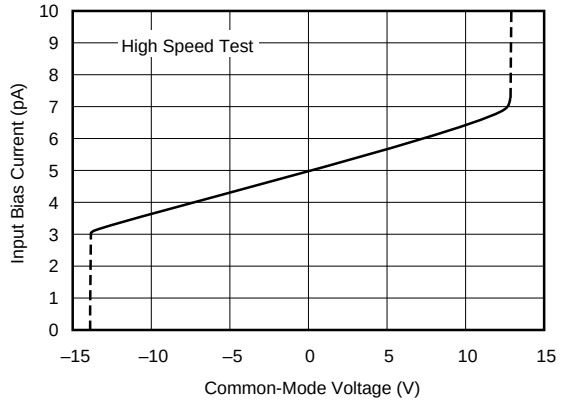
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE



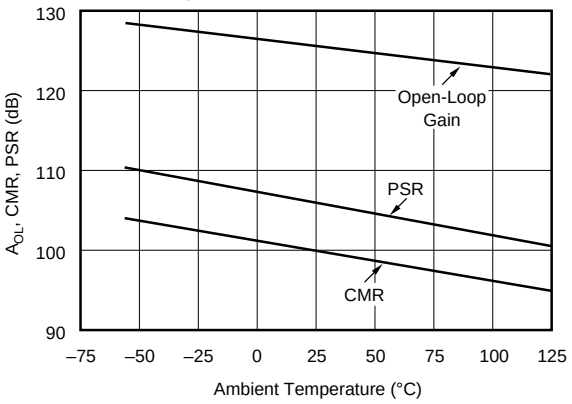
INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE



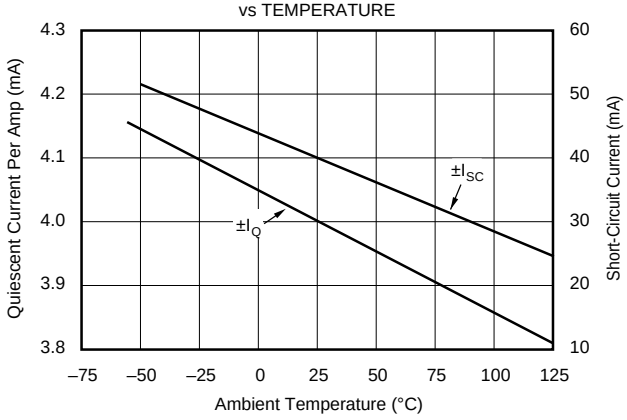
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

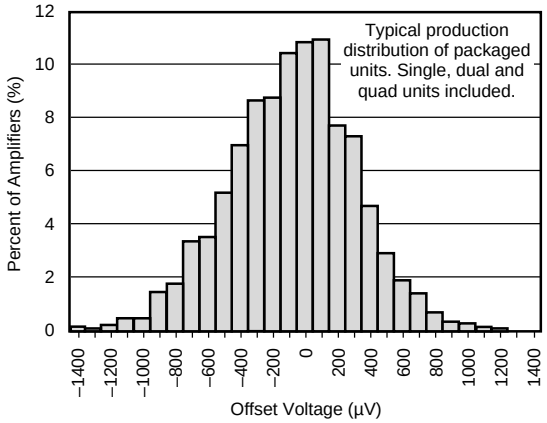
A_{OL}, CMR, PSR vs TEMPERATURE



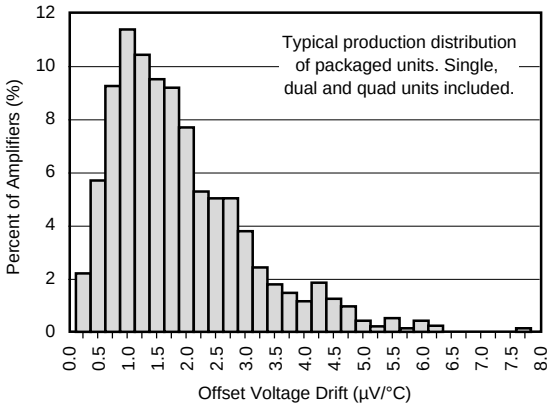
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



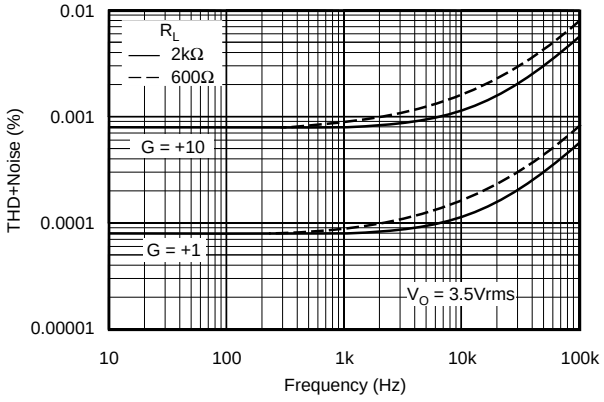
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



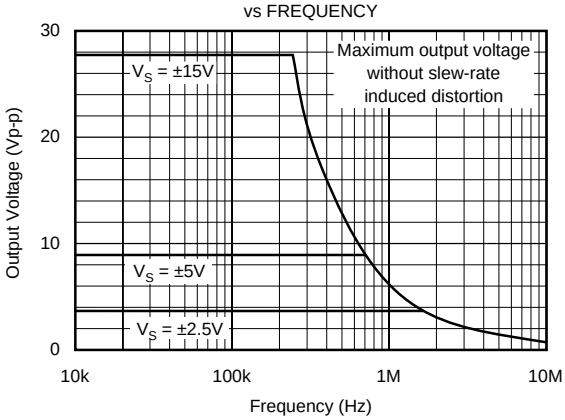
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



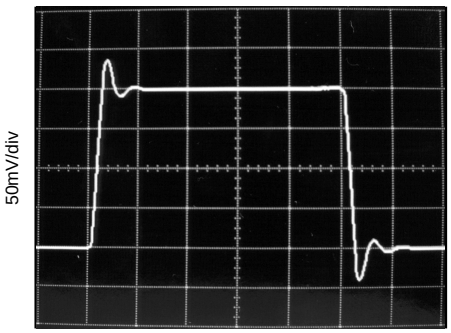
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



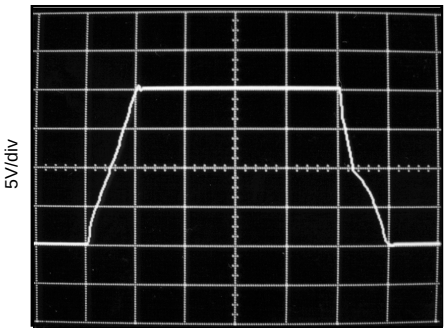
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

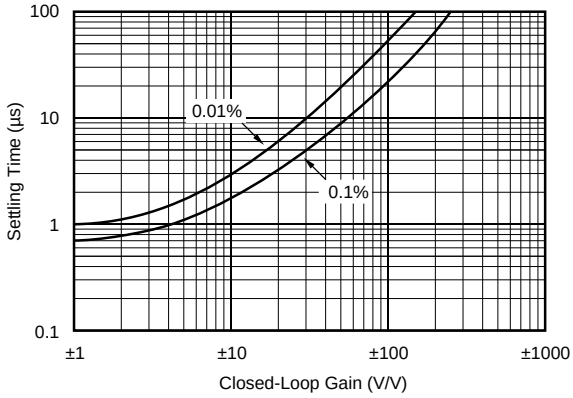
SMALL-SIGNAL STEP RESPONSE
G =1, C_L = 100pF



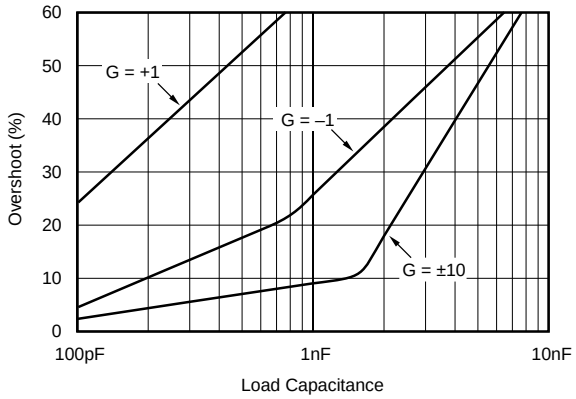
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



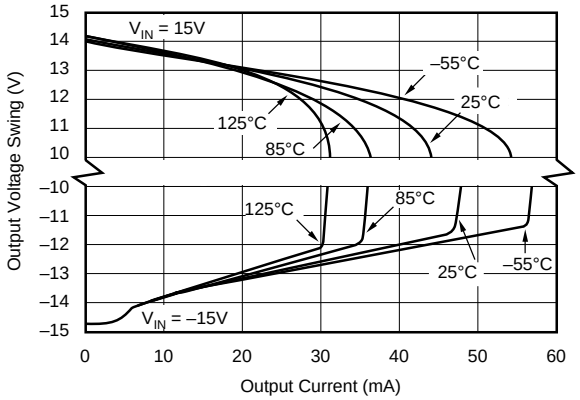
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

OPA132 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA132 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA132 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA132 series op amps operate with power supplies from ±2.5V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA132 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA132 (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

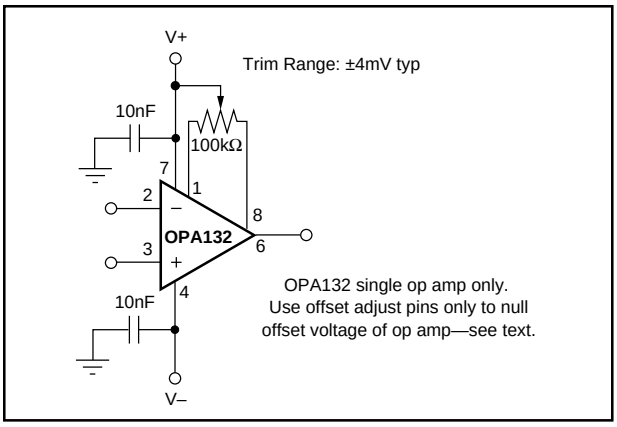


FIGURE 1. OPA132 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The FET-inputs of the OPA132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input op amps increases with temperature as shown in the typical performance curve "Input Bias Current vs Temperature."

The OPA132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±3V supplies reduces power dissipation to one-fifth that at ±15V.

The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA}. Refer to the specifications table.

Circuit board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA132 series. See the typical performance curve "Input Bias Current vs Common-Mode Voltage."