

LM13600

Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

Features

- g_m adjustable over 6 decades
- Excellent g_m linearity

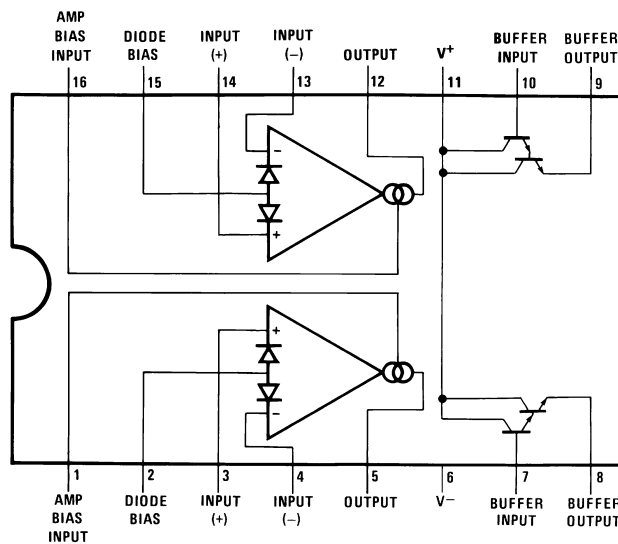
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



DS007980-2

Top View

Order Number LM13600M, LM13600N or LM13600AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)

LM13600	36 V _{DC} or ±18V
LM13600A	44 V _{DC} or ±22V

Power Dissipation (Note 3) T_A = 25°C 570 mW

Differential Input Voltage ±5V

Diode Bias Current (I_D) 2 mAAmplifier Bias Current (I_{ABC}) 2 mA

Output Short Circuit Duration Continuous

Buffer Output Current (Note 4) 20 mA

Operating Temperature Range 0°C to +70°C

DC Input Voltage +V_S to -V_S

Storage Temperature Range -65°C to +150°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds) 260°C

Small Outline Package

Vapor Phase (60 seconds) 215°C

Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 5)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V _{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I _{ABC} = 5 µA		0.3	4		0.3	1	mV
V _{OS} Including Diodes	Diode Bias Current (I _D) = 500 µA		0.5	5		0.5	2	mV
Input Offset Change	5 µA ≤ I _{ABC} ≤ 500 µA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	µA
Input Bias Current			0.4	5		0.4	5	µA
	Over Specified Temperature Range		1	8		1	7	µA
Forward Transconductance (g _m)		6700	9600	13000	7700	9600	12000	µmho
	Over Specified Temperature Range	5400			4000			µmho
g _m Tracking			0.3			0.3		dB
Peak Output Current	R _L = 0, I _{ABC} = 5 µA		5		3	5	7	µA
	R _L = 0, I _{ABC} = 500 µA	350	500	650	350	500	650	µA
	R _L = 0, Over Specified Temp Range	300			300			µA
Peak Output Voltage								
	Positive	+12	+14.2		+12	+14.2		V
Negative		-12	-14.4		-12	-14.4		V
	R _L = ∞, 5 µA ≤ I _{ABC} ≤ 500 µA							
Supply Current	I _{ABC} = 500 µA, Both Channels		2.6			2.6		mA
V _{OS} Sensitivity								
	Positive		20	150		20	150	µV/V
Negative			20	150		20	150	µV/V
	Δ V _{OS} /Δ V-							
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 6) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	I _{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	I _{ABC} = 0 (Refer to Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		kΩ
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/µs
Buffer Input Current	(Note 6), Except I _{ABC} = 0 µA		0.2	0.4		0.2	0.4	µA
Peak Buffer Output Voltage	(Note 6)	10			10			V

Electrical Characteristics (Note 5) (Continued)

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For selections to a supply voltage above $\pm 22\text{V}$, contact factory.

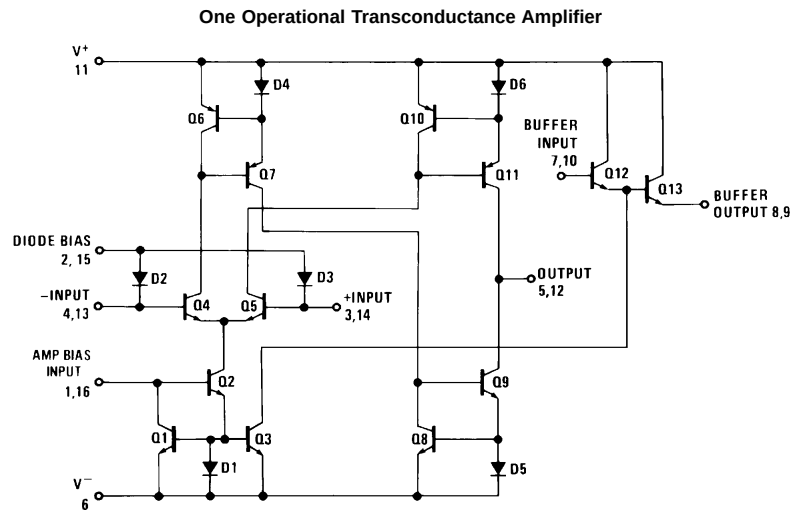
Note 3: For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

Note 4: Buffer output current should be limited so as to not exceed package dissipation.

Note 5: These specifications apply for $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, amplifier bias current (I_{ABC}) = $500\text{ }\mu\text{A}$, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 6: These specifications apply for $V_S = \pm 15\text{V}$, $I_{ABC} = 500\text{ }\mu\text{A}$, $R_{OUT} = 5\text{ k}\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

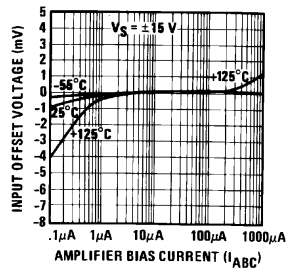
Schematic Diagram



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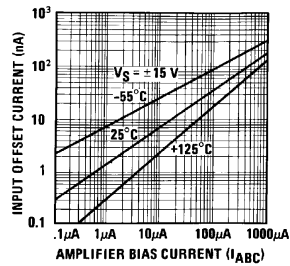
Typical Performance Characteristics

Input Offset Voltage



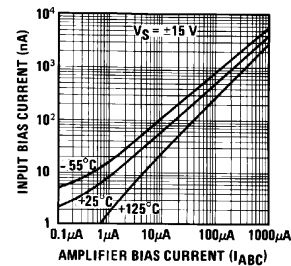
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Input Offset Current



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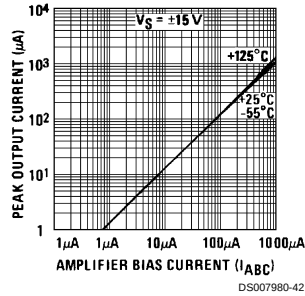
Input Bias Current



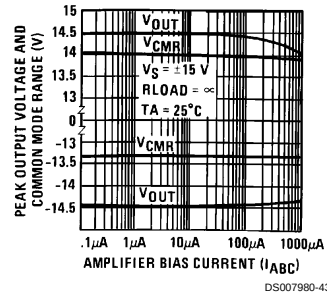
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Typical Performance Characteristics (Continued)

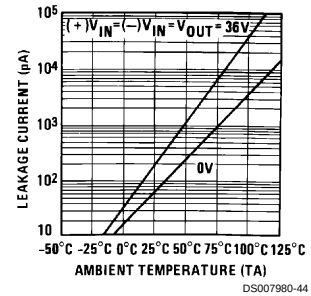
Peak Output Current



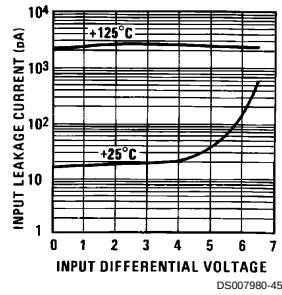
Peak Output Voltage and Common Mode Range



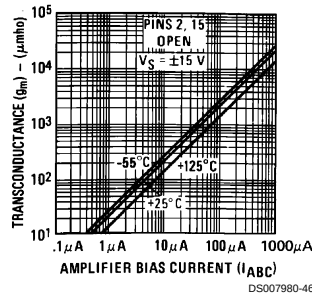
Leakage Current



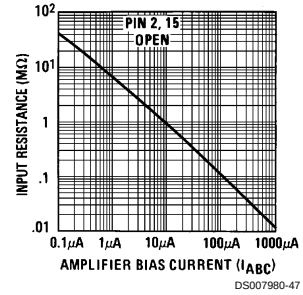
Input Leakage



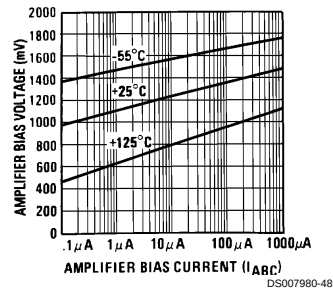
Transconductance



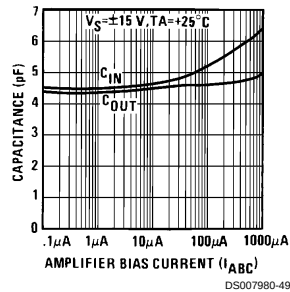
Input Resistance



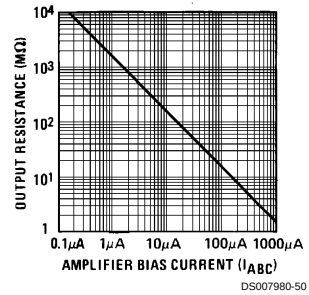
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance

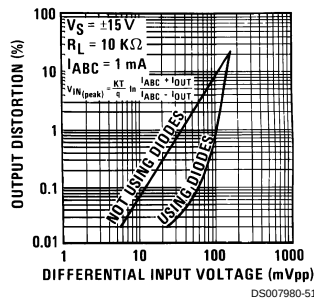


Output Resistance

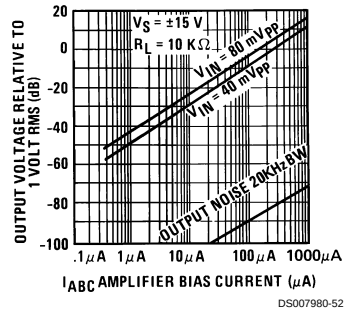


Typical Performance Characteristics (Continued)

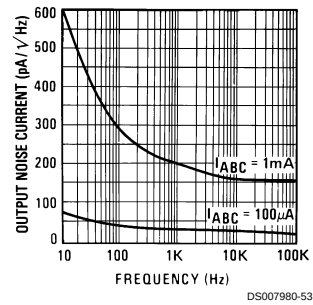
Distortion vs Differential Input Voltage



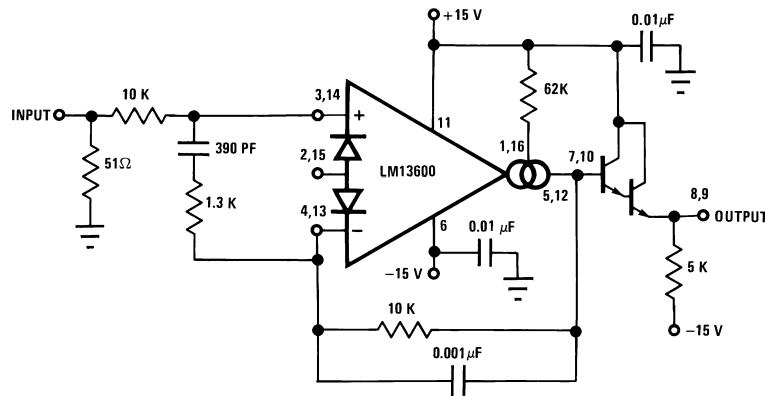
Voltage vs Amplifier Bias Current



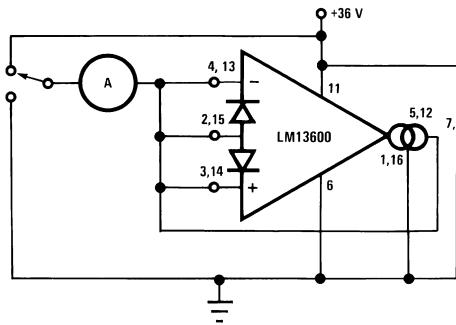
Output Noise vs Frequency



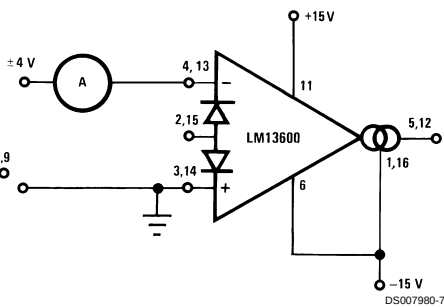
Unity Gain Follower



Leakage Current Test Circuit



Differential Input Current Test Circuit



Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and $Q_{1,3}$, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC} :

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the $\ln$ function can be approximated as:

$$\begin{aligned} \frac{kT}{q} \ln \frac{I_5}{I_4} &\approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \\ I_4 &\approx I_5 \approx \frac{I_{ABC}}{2} \end{aligned} \quad (3)$$

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

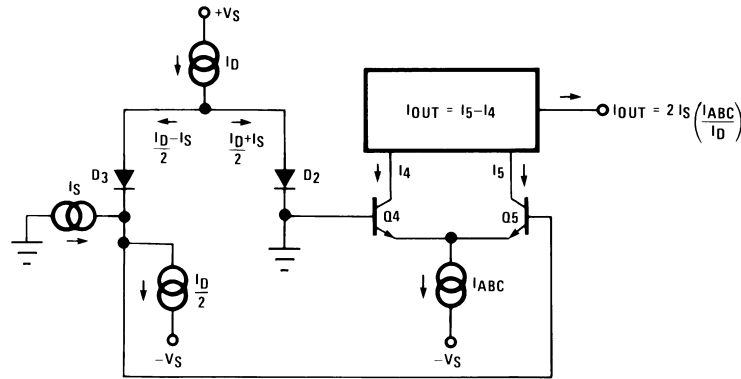


FIGURE 1. Linearizing Diodes

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC} .

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation (3) becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S . Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT} , currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\begin{aligned} \frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} &= \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}} \\ \therefore I_{OUT} &= I_S \left(\frac{2I_{ABC}}{I_D} \right) \text{ for } |I_S| < \frac{I_D}{2} \end{aligned} \quad (6)$$

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Applications-Voltage Controlled Amplifiers (Continued)

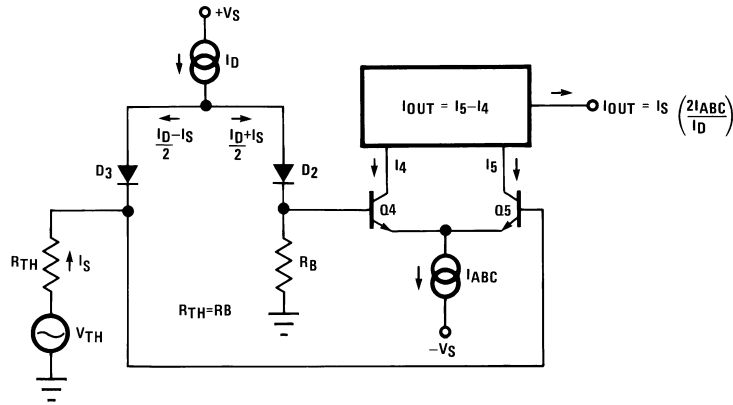


FIGURE 3. Equivalent VCA Input Circuit

Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D} (I_{ABC}) = \frac{-2I_S}{I_D} \frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D} \frac{(V^- + 1.4V)}{R_C}$$

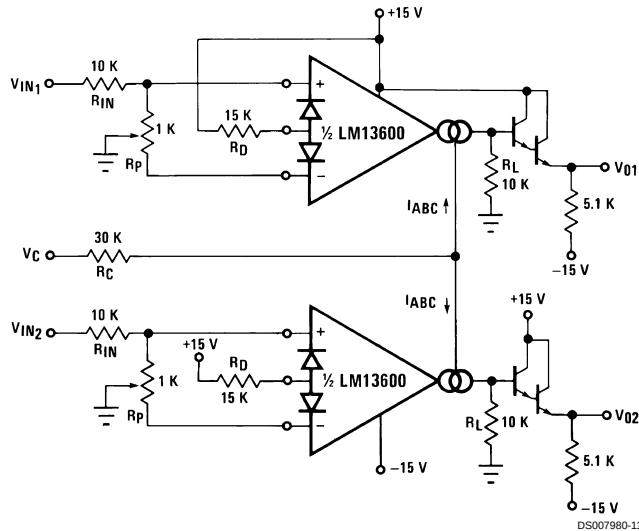
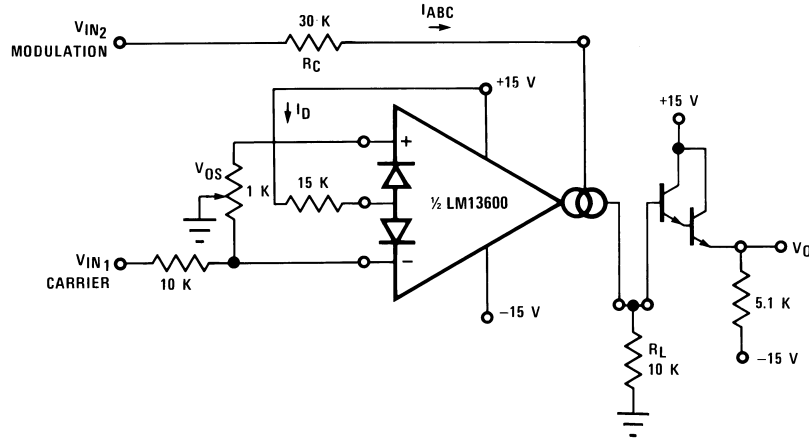


FIGURE 4. Stereo Volume Control

Stereo Volume Control (Continued)



DS007980-12

FIGURE 5. Amplitude Modulator

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2$ ($V^- + 1.4V$) into I_O . The circuit of Figure 6 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O . Noting that the gain of the LM13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC} , Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3 V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

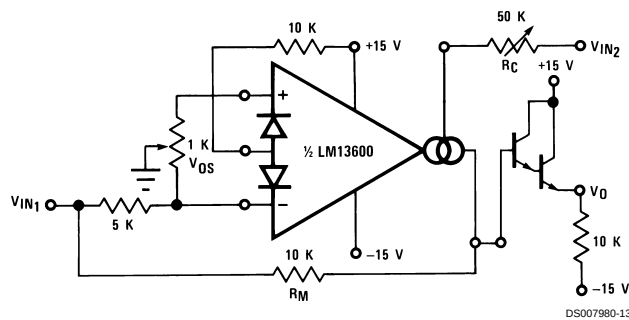
An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in

Figure 8. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{9m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at $25^\circ C$. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.



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FIGURE 6. Four-Quadrant Multiplier

Voltage Controlled Resistors (Continued)

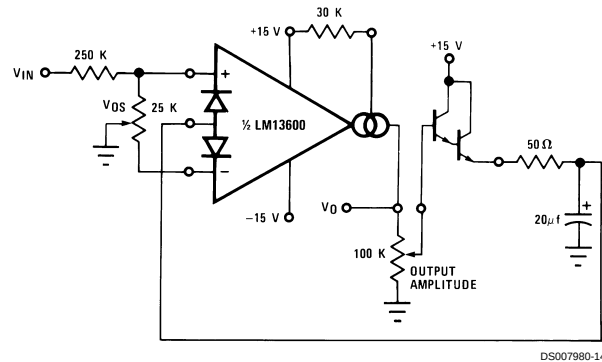


FIGURE 7. AGC Amplifier

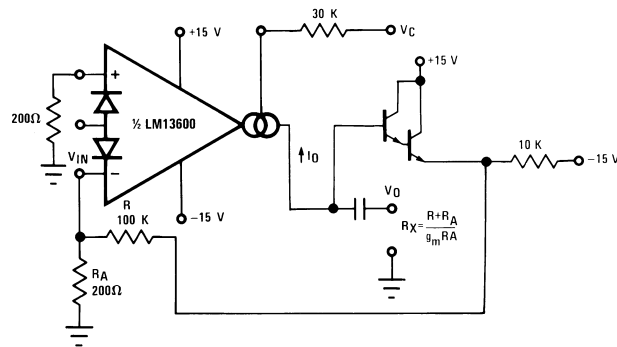


FIGURE 8. Voltage Controlled Resistor, Single-Ended

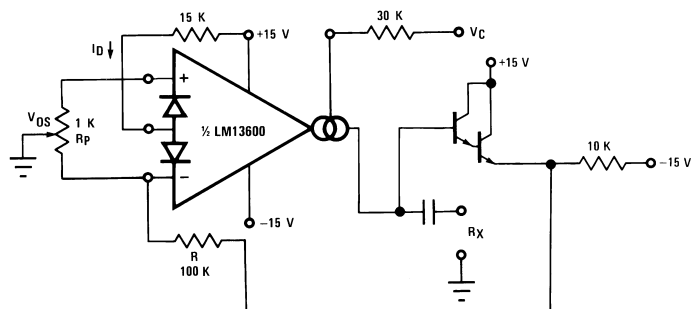
Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A) . At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation, where

g_m is again $19.2 \times I_{ABC}$ at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

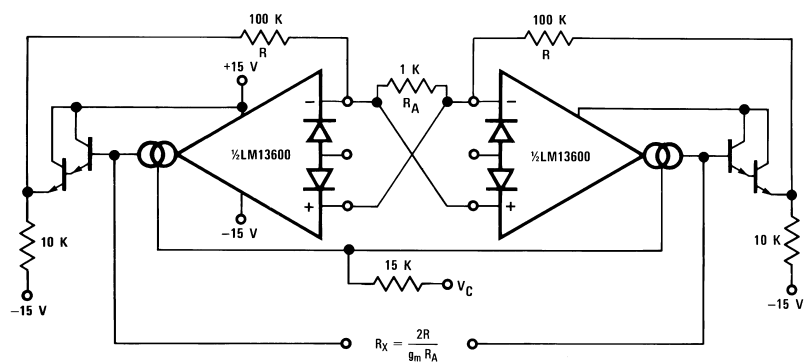
Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlington, these filters perform well over several decades of frequency.

Voltage Controlled Filters (Continued)



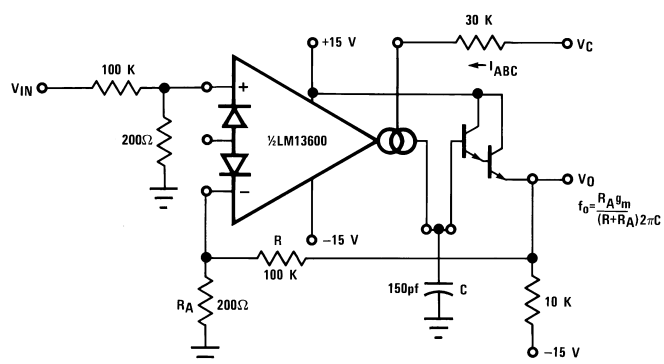
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FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes



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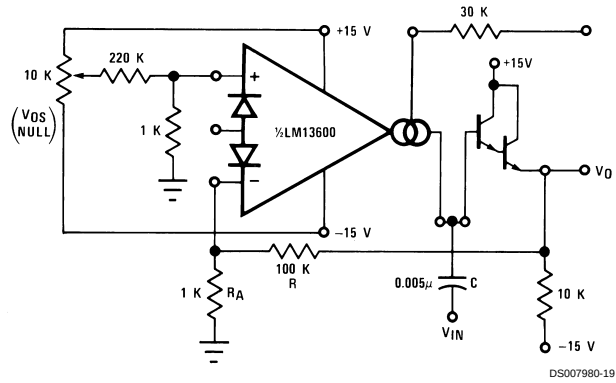
FIGURE 10. Floating Voltage Controlled Resistor



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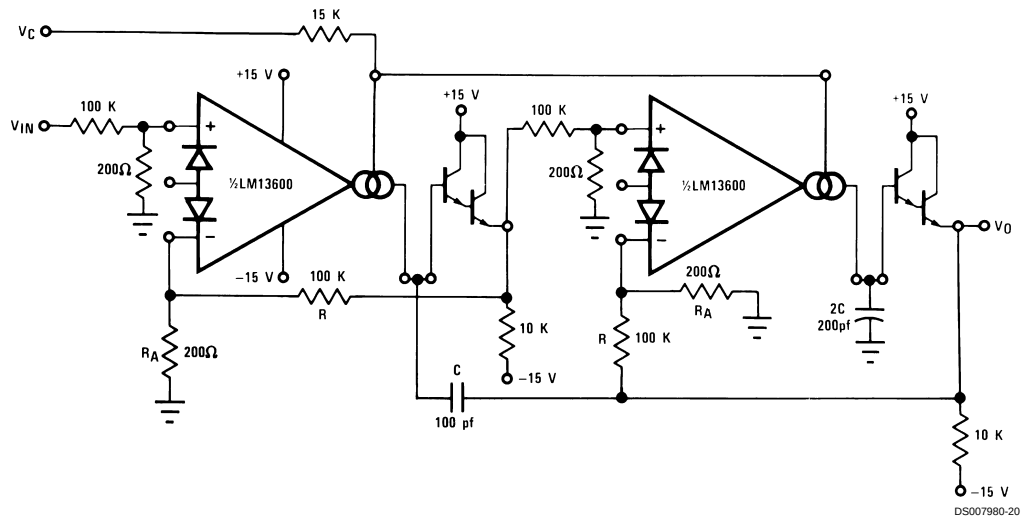
FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)



$$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$$

FIGURE 12. Voltage Controlled Hi-Pass Filter



$$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$$

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

Voltage Controlled Filters (Continued)

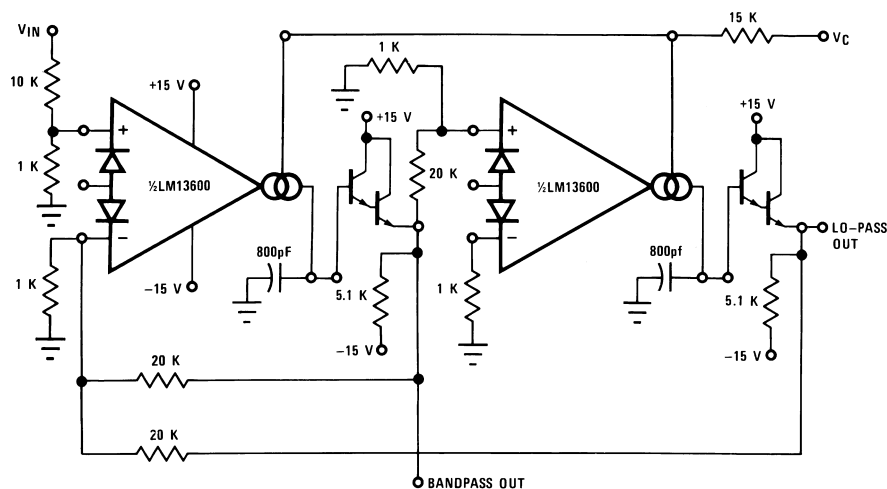


FIGURE 14. Voltage Controlled State Variable Filter

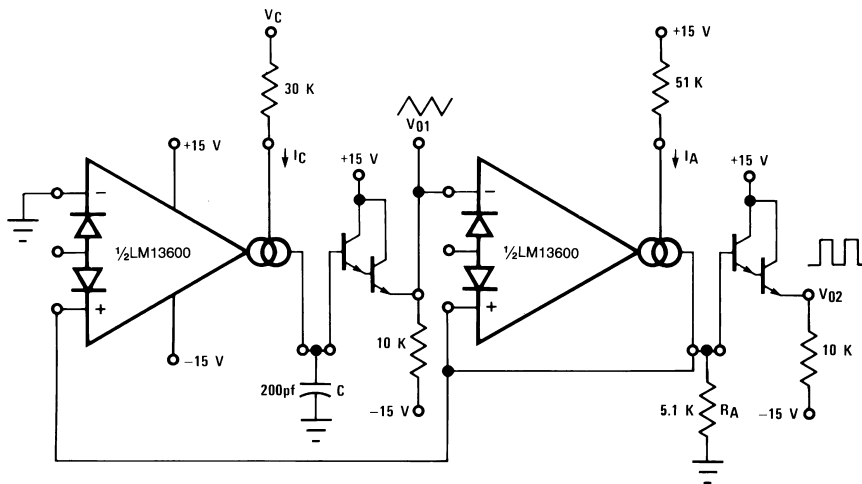
Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C .

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

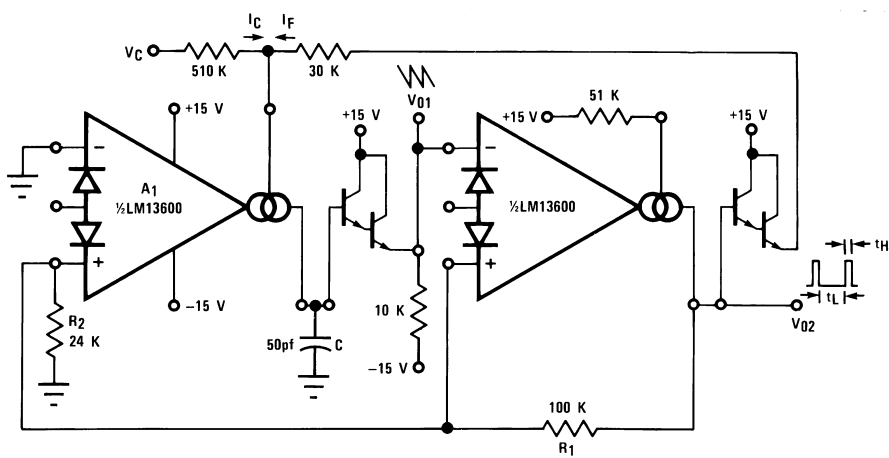
Voltage Controlled Oscillators (Continued)



DS007980-22

$$f_{OSC} = \frac{I_C}{4C_{I_A}R_A}$$

FIGURE 15. Triangular/Square-Wave VCO



DS007980-23

$$V_{PK} = \frac{(V^+ - 0.8V)R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_E}$$

$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_o \approx \frac{I_C}{2V_{PKC}} \text{ for } I_C \ll I_F$$

FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)

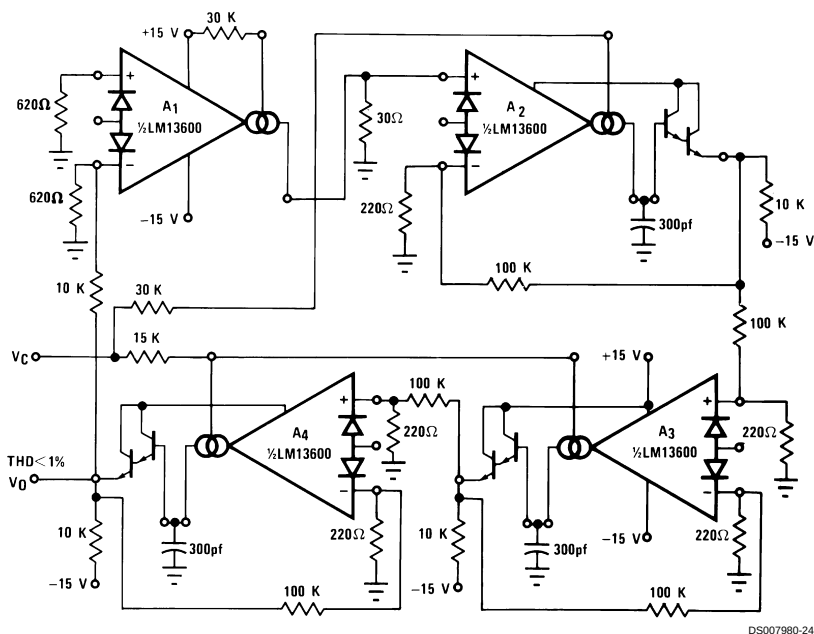


FIGURE 17. Sinusoidal VCO

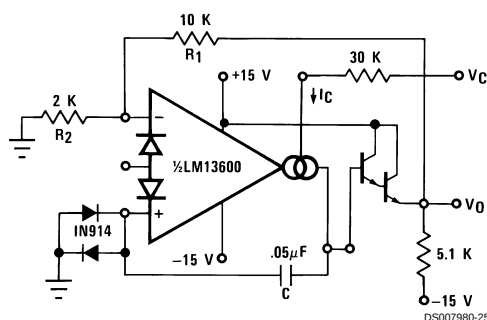


FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 .

when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_{O_1} , can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O . C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13600 slew rate into 150 pF when the $(V_{IN1}-V_{IN2})$ differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a $\pm 5\%$ hold-in range and an input sensitivity of about 300 mV.

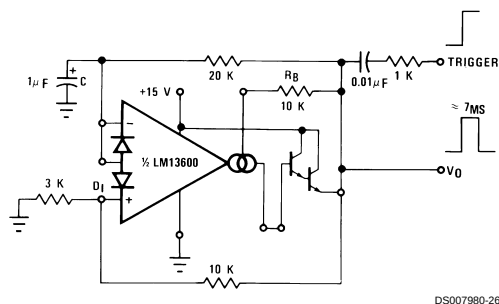


FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)

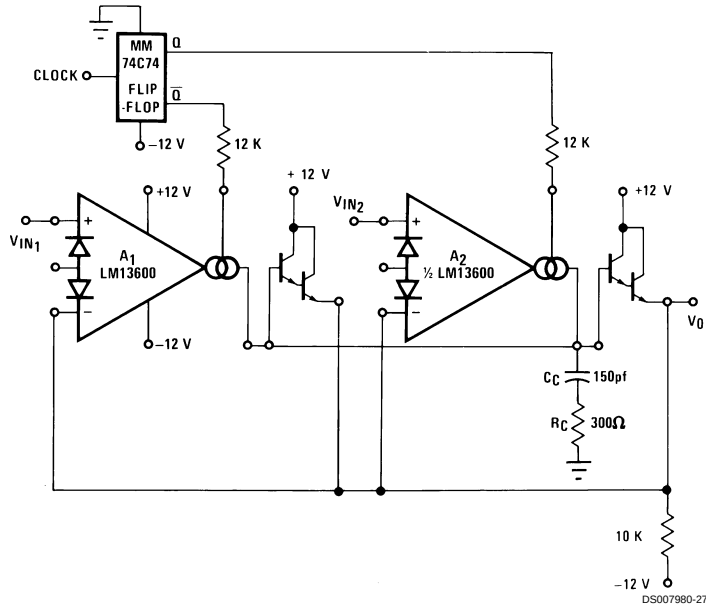


FIGURE 20. Multiplexer

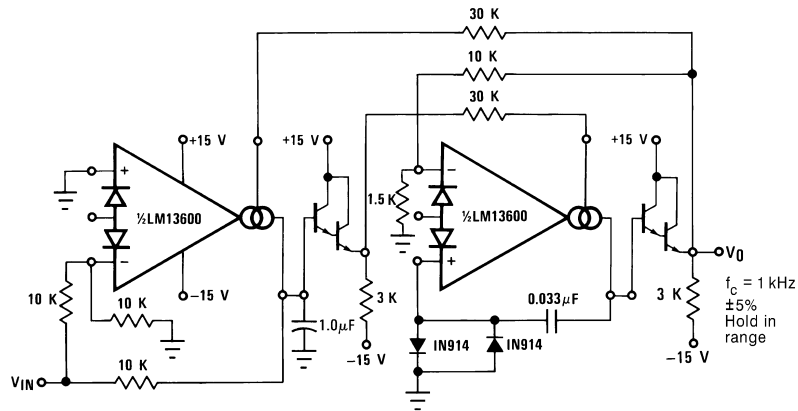


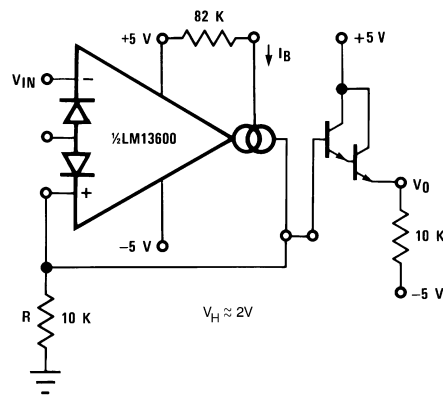
FIGURE 21. Phase Lock Loop

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L) C_1$ is sourced into C_1 and R_1 . This once-per-cycle charge is then balanced by the current of V_O/R_1 . The maximum f_{IN} is limited by the amount of time required to charge C_1 from V_L to V_H with a current of I_B , where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_1 when A1 switches low.

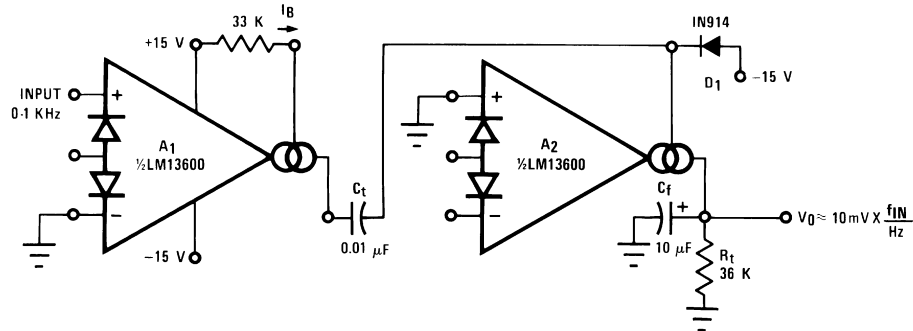
The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O . A1 then charges storage capacitor C to hold V_O equal to V_{INPK} . One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)



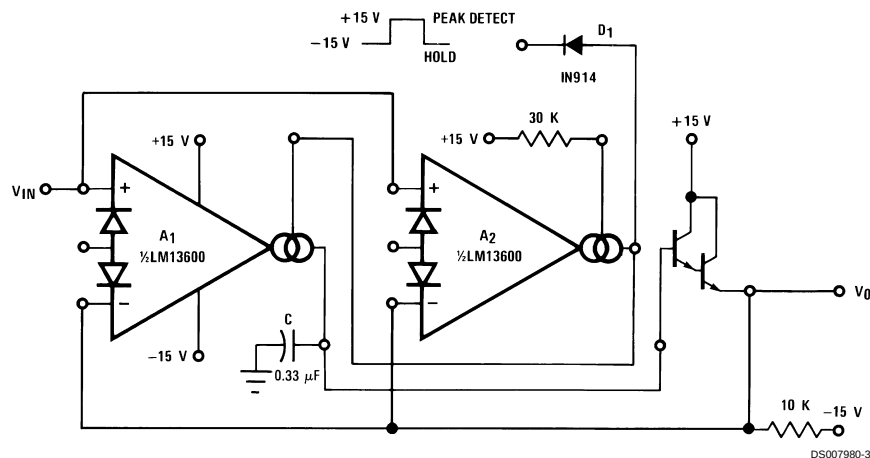
DS007980-29

FIGURE 22. Schmitt Trigger



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FIGURE 23. Tachometer



DS007980-31

FIGURE 24. Peak Detector and Hold Circuit

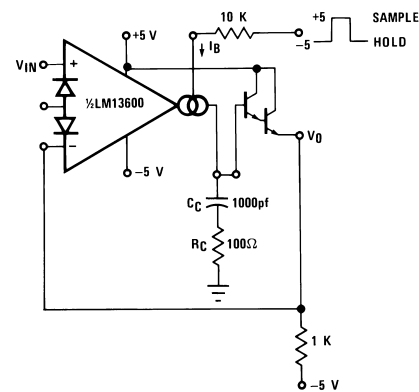
The Sample-and-Hold circuit of Figure 25 also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on

continuously. The Ramp-and-Hold of Figure 26 sources I_B

Additional Applications (Continued)

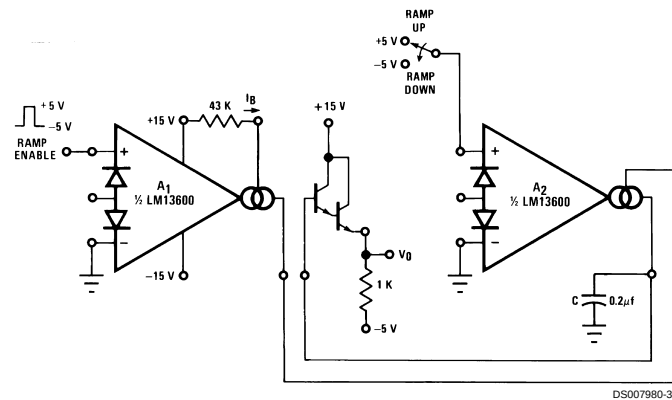
into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.



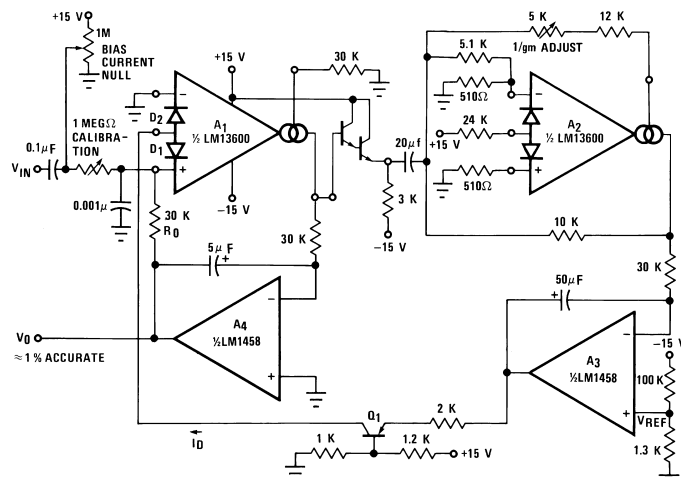
DS007980-32

FIGURE 25. Sample-Hold Circuit



DS007980-33

FIGURE 26. Ramp and Hold



DS007980-34

FIGURE 27. True RMS Converter

Additional Applications (Continued)

The circuit of *Figure 28* is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of *Figure 29* responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 30*.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 31* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its linear range. From *Equation (5)*, the input voltage to A1 is:

$$V_{IN1} = \frac{-2kT I_3}{q I_2} = \frac{2kT V_C}{q I_2 R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2) V_{IN1}}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B1} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp \left[\frac{2(R_1 + R_2) V_C}{R_1 I_2 R_C} \right]$$

This logarithmic current can be used to bias the circuit of *Figure 4* provide a temperature independent stereo attenuation characteristic.

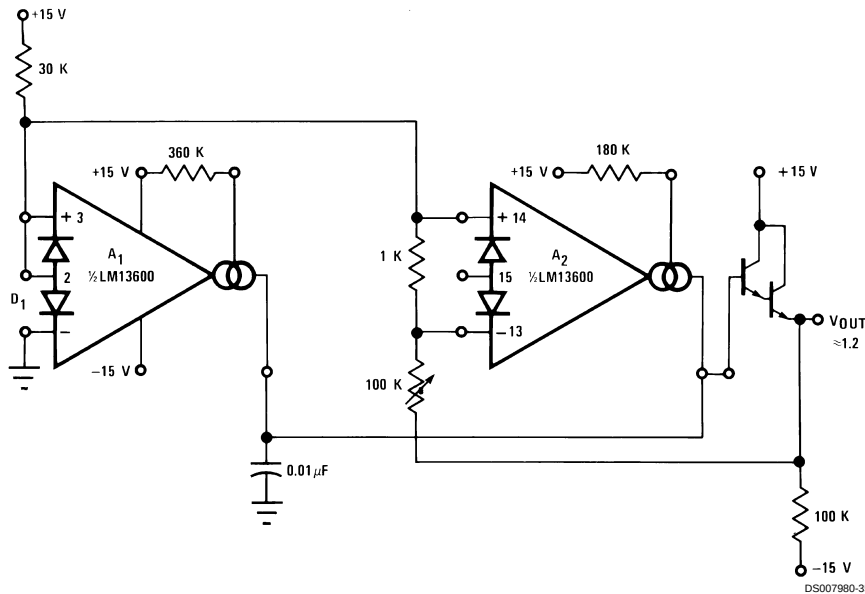
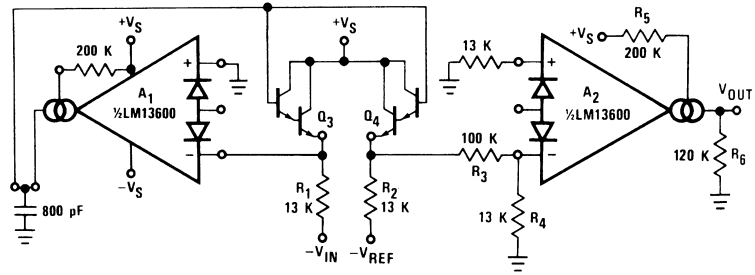


FIGURE 28. Delta VBE Reference

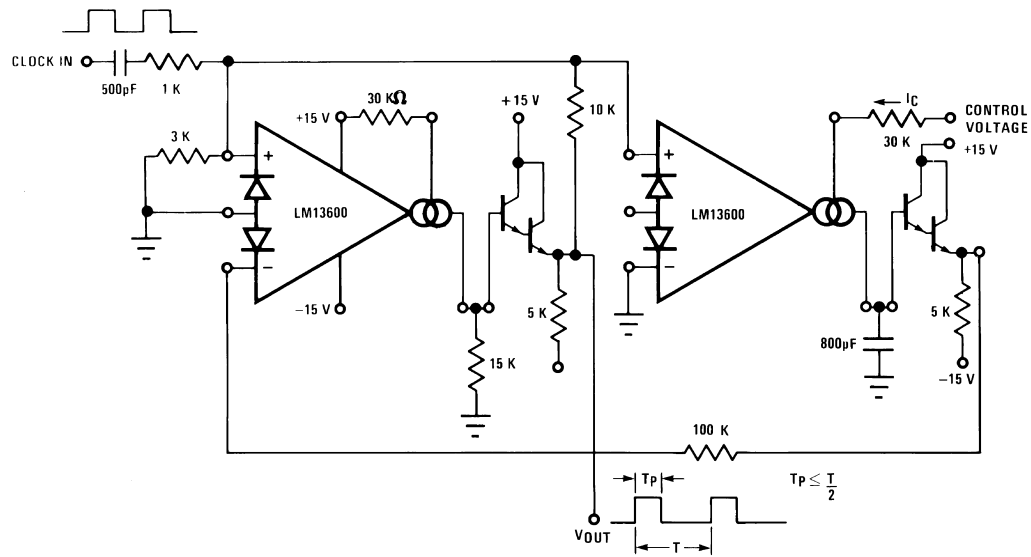
Additional Applications (Continued)



DS007980-36

$$V_{OUT} = \frac{(2V_S - 1.2V)(R_4)(R_6)}{(R_3 + R_4)(R_5)} \ln \frac{V_{IN} R_2}{V_{REF} R_1}$$

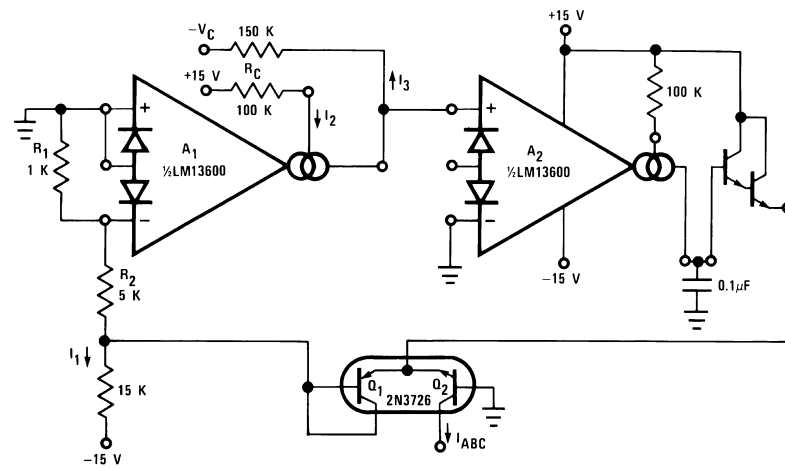
FIGURE 29. Log Amplifier



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FIGURE 30. Pulse Width Modulator

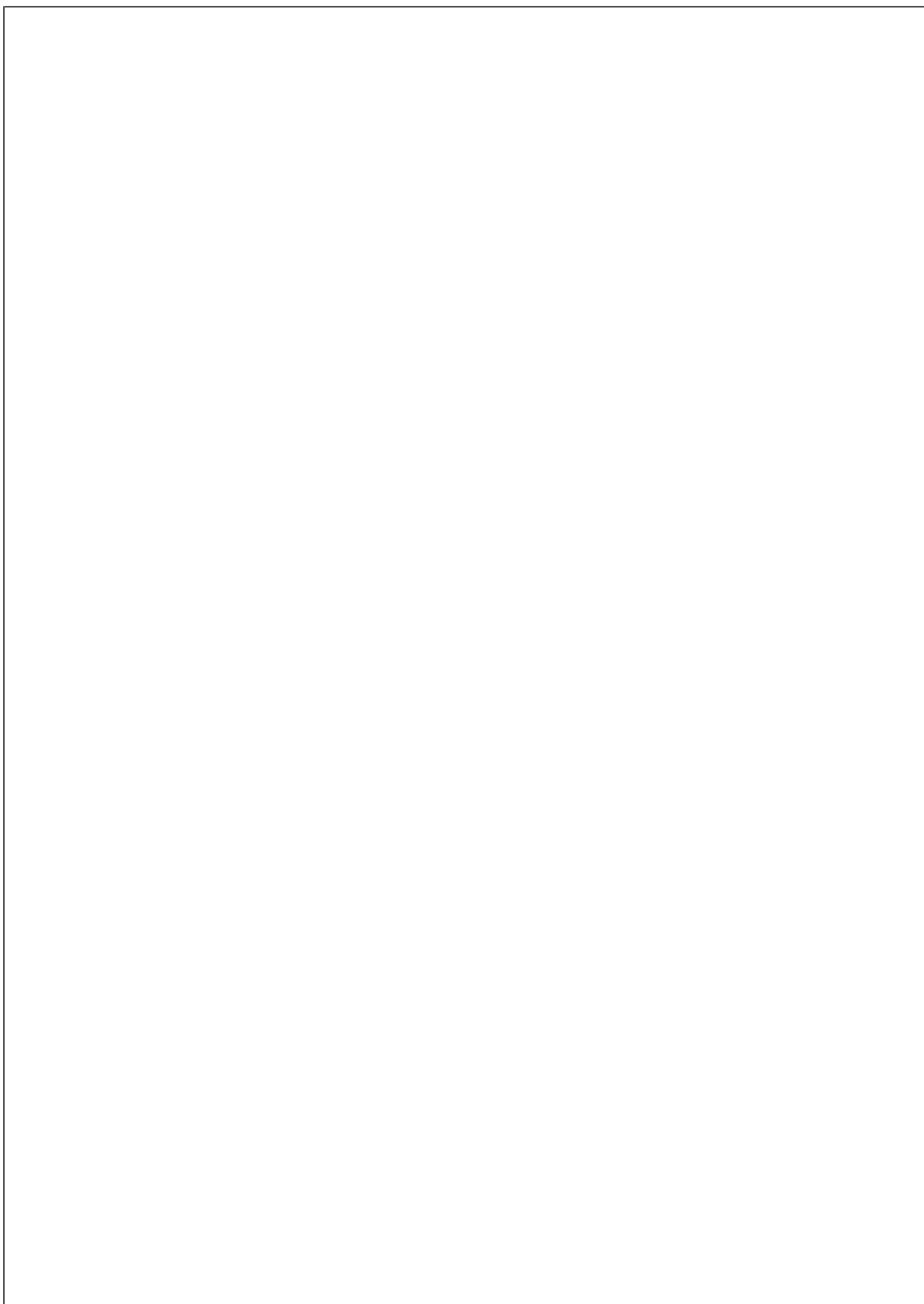
Additional Applications (Continued)



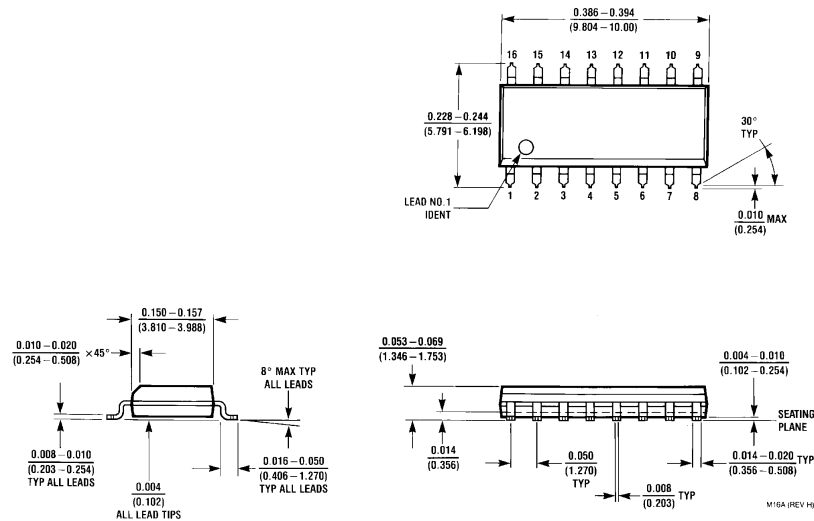
DS007980-38

$$I_{ABC} = I_1 \exp \left[\frac{-CI_3}{I_2} \right]$$

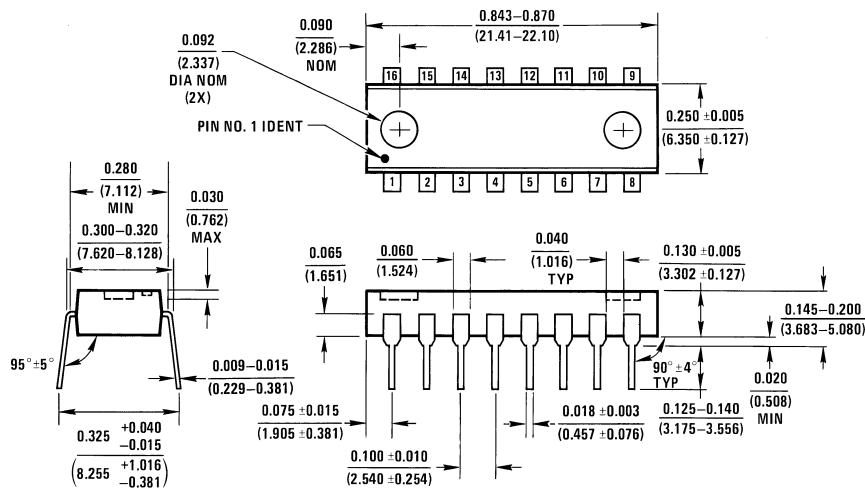
FIGURE 31. Logarithmic Current Source



Physical Dimensions inches (millimeters) unless otherwise noted



S.O. Package (M)
Order Number LM13600M
NS Package Number M16A



Molded Dual-In-Line Package (N)
Order Number LM13600N or LM13600AN
NS Package Number N16A

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